

ABSTRACT OF THE DISCLOSURE

Capacitors, DRAM circuitry, and methods of forming the same are described. In one embodiment, a capacitor comprises a first container which is joined with a substrate node location and has an opening defining a first interior area. A second container is joined with the node location and has an opening defining a second interior area. The areas are spaced apart from one another in a non-overlapping relationship. A dielectric layer and a conductive capacitor electrode layer are disposed operably proximate the first and second containers. In another embodiment, the first and second containers are generally elongate and extend away from the node location along respective first and second central axes. The axes are different and spaced apart from one another. In yet another embodiment, a conductive layer of material is disposed over and in electrical communication with a substrate node location. The layer of material has an outer surface with a first region and a second region spaced apart from the first region. A first container is formed over and in electrical communication with the first region and a second container is formed over and in electrical communication with the second region. In yet another embodiment, the first and second containers define container volumes which are discrete and separated from one another.